

### Schemas Change History

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[illegible]

**CAD Note:**

Property: BUILD-OPT

ALL = Installed Part.

DNP = Not Installed Part.

DBG\_D = EV/DV phase only

DBG\_S = Short after design fixed

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stack up 6L 0.8mm+/-0.1mm: 1-4-1+			Impedance					
Layer	material	1-4-1+		L3( refer L2and L4)	L4(refer L3 and L5)	L5(refer L4 and L6)	L1(refer L2)	L6(refer L5)
Top Surface	soldermask	0.8	Target Impedance	Trace Width (mil)	Trace Width (mil)	Trace Width (mil)	Trace Width (mil)	Trace Width (mil)
L1-Component/GND	1/3oz+plating	1.2	Single-end, 50Ω±10%	2.3	2.3	1.6	4.25	4.25
	PP:EM-285B 1080	2.71	Single-end, 45Ω±5Ω	2.9	2.9	2	5.25	5.25
L2-GND	1/3oz+plating	1.1	Single-end, 42.5Ω±5Ω	3.35	3.35	2.3	5.9	5.9
	PP:EM-285B 1067	1.81	Single-end, 40Ω±5Ω	3.7	3.7	2.5	6.6	6.6
L3-Signal/Impedance	1oz	1.3	Single-end, 25Ω±5Ω	8.3	8.3	5.8	14	14
	Core:EM-285 14mil	14	unit :mil	Width / Space	Width / Space	Width / Space	Width / Space	Width / Space
L4-Signal/Impedance	1oz	1.3	Differential, 100Ω±15%	2.2/8.8	2.2/8.8	1.55/10	3/4.5	3/4.5
	PP:EM-285B 1067	1.81	Differential, 90Ω±10%	2.7/8.3	2.7/8.3	2/8	4.1/5	4.1/5
L5-PWR	1/3oz+plating	1.1	Differential, 88Ω±10%	2.85/8.15	2.85/8.15	2.1/8	4.3/5	4.3/5
	PP:EM-285B 1080	2.71	Differential, 85Ω±10%	3.05/7.95	3.05/7.95	2.25/8	4.3/4	4.3/4
L6-Component/GND	1/3oz+plating	1.2	Differential, 70Ω±10%	4.35/6.65	4.35/6.65	3.2/5	6.9/5	6.9/5
Bottom Surface	soldermask	0.8	Differential, 50Ω±10%	7.3/4.7	7.3/4.7	5.55/5	13/8	13/8
Total		mil 31.84						
		um 808.74						

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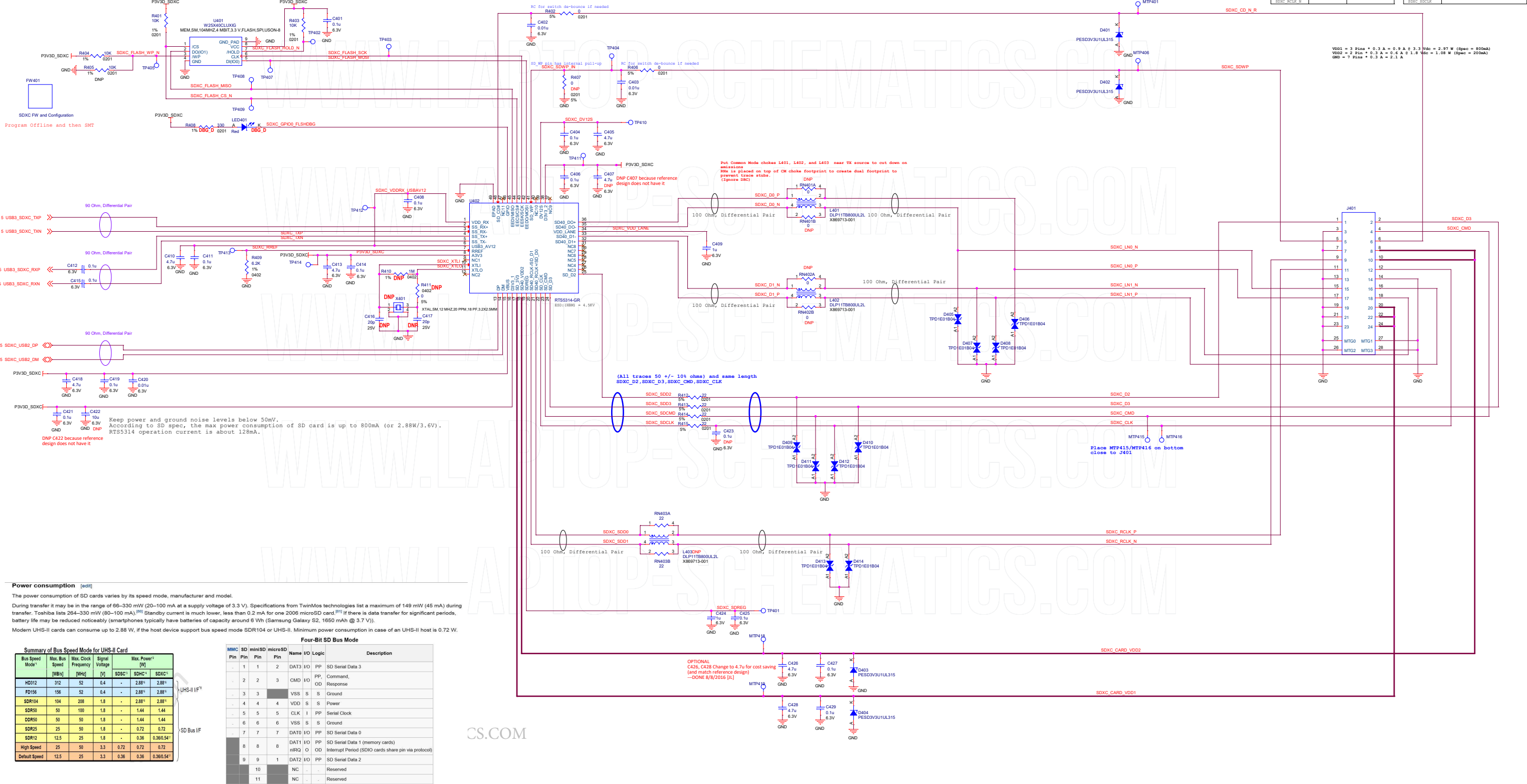


# SDXC Card Reader RTS5314

MATCHING FOR SDXC UHS2 SIGNALS				MATCHING FOR SDXC UHS1 SIGNALS			
SDXC NAME	INTERFACER (P/N)	INTERFACER (P/N)	MATCHING	SDXC NAME	INTERFACER (P/N)	INTERFACER (P/N)	MATCHING
SDXC_LAN0_P	5 M1LA			SDXC_SDO0			
SDXC_LAN0_N				SDXC_SDO1			
SDXC_LAN1_P	5 M1LA			SDXC_SDO2			
SDXC_LAN1_N				SDXC_SDO3			
SDXC_RCLK_P	5 M1LA			SDXC_SDO4			
SDXC_RCLK_N				SDXC_SDO5			

VDD1 = 3 Pins \* 0.3 A = 0.9 A @ 3.3 Vdc = 2.97 W (Spec = 800mA)  
VDD2 = 2 Pins \* 0.3 A = 0.6 A @ 1.8 Vdc = 1.08 W (Spec = 200mA)  
GND = 7 Pins \* 0.3 A = 2.1 A

Place SCK, MOSI, MISO, CS\_N test points on Bottomside



## Power consumption

The power consumption of SD cards varies by its speed mode, manufacturer and model.

During transfer it may be in the range of 66–330 mW (20–100 mA at a supply voltage of 3.3 V). Specifications from TwinMos technologies list a maximum of 149 mW (45 mA) during transfer. Toshiba lists 264–330 mW (80–100 mA).<sup>[8]</sup> Standby current is much lower, less than 0.2 mA for one 2008 microSD card.<sup>[8]</sup> If there is data transfer for significant periods, battery life may be reduced noticeably (smartphones typically have batteries of capacity around 6 Wh (Samsung Galaxy S2, 1650 mAh @ 3.7 V)).

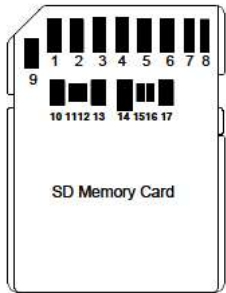
Modern UHS-II cards can consume up to 2.88 W, if the host device supports bus speed mode SDR104 or UHS-II. Minimum power consumption in case of an UHS-II host is 0.72 W.

Summary of Bus Speed Mode for UHS-II Card						
Bus Speed Mode <sup>1</sup>	Max. Bus Speed [MB/s]	Max. Clock Frequency [MHz]	Signal Voltage [V]	SDSC <sup>1</sup>	SDHC <sup>1</sup>	SDXC <sup>1</sup>
HD312	312	52	0.4	-	2.88 <sup>1</sup>	2.88 <sup>1</sup>
FD156	156	52	0.4	-	2.88 <sup>1</sup>	2.88 <sup>1</sup>
SDR104	104	208	1.8	-	2.88 <sup>1</sup>	2.88 <sup>1</sup>
SDR50	50	100	1.8	-	1.44	1.44
DDR50	50	50	1.8	-	1.44	1.44
SDR25	25	50	1.8	-	0.72	0.72
SDR12	12.5	25	1.8	-	0.36	0.36/0.54 <sup>2</sup>
High Speed	25	50	3.3	0.72	0.72	0.72
Default Speed	12.5	25	3.3	0.36	0.36	0.36/0.54 <sup>2</sup>

Four-Bit SD Bus Mode							
MMC Pin	SD Pin	miniSD Pin	microSD Pin	Name	I/O	Logic	Description
1	1	2	2	DAT3	I/O	PP	SD Serial Data 3
2	2	3	3	CMD	I/O	PP, OD	Command, Response
3	3			VSS	S	S	Ground
4	4	4	4	VDD	S	S	Power
5	5	5	5	CLK	I	PP	Serial Clock
6	6	6	6	VSS	S	S	Ground
7	7	7	7	DAT0	I/O	PP	SD Serial Data 0
	8	8	8	DAT1	I/O	PP	SD Serial Data 1 (memory cards)
				OD			Interdigit Period (SDIO cards share pin via protocol)
9	9	1		DAT2	I/O	PP	SD Serial Data 2
		10		NC	-	-	Reserved
				NC	-	-	Reserved

## UHS-II Interface Pad Assignment

Pin #	Name	Type	Description
4	VDD1	Supply voltage	2.7V to 3.6V
7	RCLK+	Differential Signaling: Input	Clock Input
8	RCLK-	Differential Signaling: Input	Clock Input
10	VSS3	Ground	
11	D0+	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
12	D0-	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.70V to 1.95V
15	D1-	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
16	D1+	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
17	VSS5	Ground	



UHS-II Card Shape and Interface (Top View)

## SD CARD CIRCUIT :

WITH OUT CARD		CARD INSERTED WRITE PROTECT : LOCK		CARD INSERTED WRITE PROTECT : UNLOCK	
W/P (#1)	GND (#21)	W/P (#1)	GND (#21)	W/P (#1)	GND (#21)
C/D1 (#12)	VSS (#11)	C/D1 (#12)	VSS (#11)	C/D1 (#12)	VSS (#11)

Frequency	12 MHz
Frequency Tolerance	±30 ppm
Effective Series Resistance	60Ωmax
Drive level	100uW
Load Capacitance(CL)	16~22pF

## UHS-II Card Operation Modes

### SD Bus Interface Modes

- DS - Default Speed up to 25MHz 3.3V signaling
- HS - High Speed up to 50MHz 3.3V signaling
- SDR12 - SDR up to 25MHz 1.8V signaling
- SDR25 - SDR up to 50MHz 1.8V signaling
- SDR50 - SDR up to 100MHz 1.8V signaling
- SDR104 - SDR up to 208MHz 1.8V signaling (Optional)
- DDR50 - DDR up to 50MHz 1.8V signaling (Optional for Standard Size Card)

### UHS-II Interface Modes

- FD156 - Full Duplex mode up to 156MB/s at 52MHz in Range B
- HD312 - Half Duplex with 2 Lanes mode up to 312MB/s in Range B (Optional)



# USB 3.0 Hub GL3523

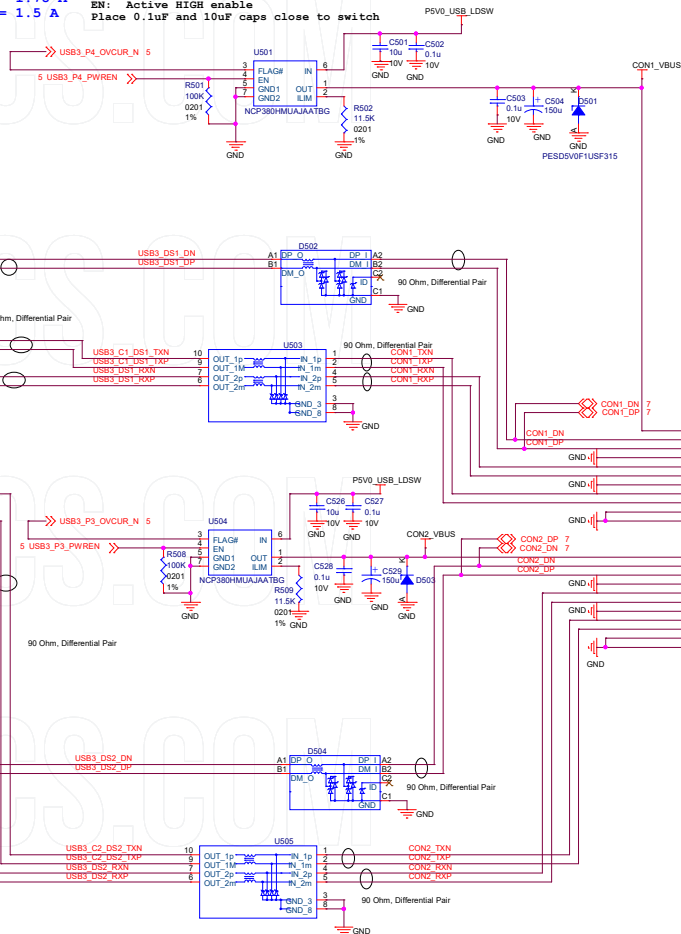
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Note that the width of the noise pulses is equal to the phase shift between the two signals, and can be translated into a time difference for a given frequency. This time difference, also known as intra-pair skew, is specified by DisplayPort as 20 ps. The recommended board trace for intra-pair skew is no more than 5 mils (0.127 mm). Ideally, all signal pairs should be of equal length to ensure zero time difference. DisplayPort, however, allows for a maximum inter-pair skew, the time difference between signal pairs, of 2 UI. The UI for high bit rate (2.7Gbps/lane) is 370 ps (nominal).

2UI = 2\*370ps = 740ps skew  
FR4 (Inner Layer) => 160ps/in  
FR4 (Outer Layer) => 150ps/in

**R = 11.5 K**  
**I(Max) = 2.05 A**  
**I(Typ) = 1.78 A**  
**I(Min) = 1.5 A**

**NCP380 Load Switch:**  
Active Discharge built in.  
FAULTn: Active-low open-drain output, asserted during overcurrent, over-temperature, or reverse-voltage conditions.  
EN: Active HIGH enable  
Place 0.1uF and 10uF caps close to switch



## IO to SL Board to Board Connector

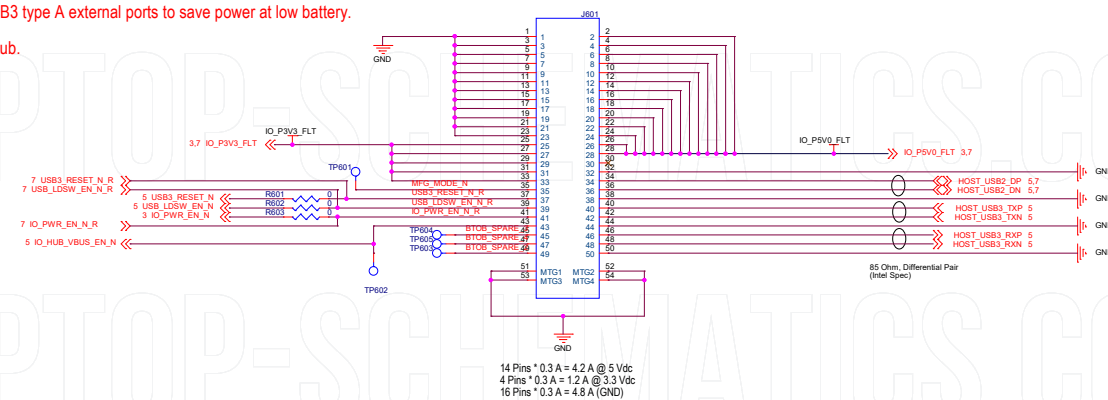
IO\_PWR\_EN\_N = SAM JR signal to disable all IO board functionality (removes all power)

USB\_LDSW\_EN\_N = Power down both USB3 type A external ports to save power at low battery.

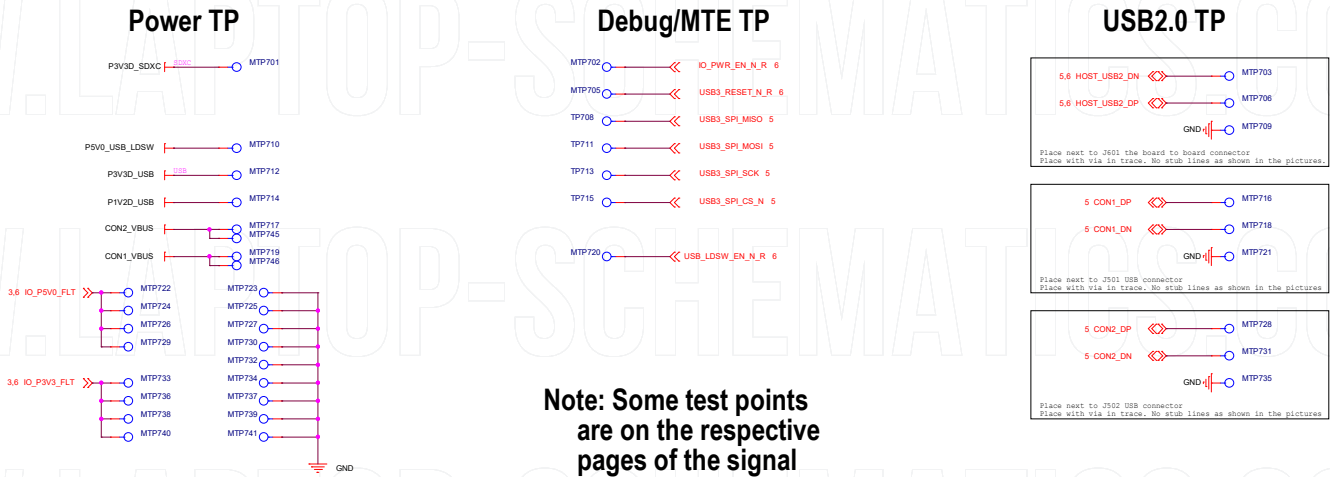
USB3\_RESET\_N = Reset USB 3.0 4 port hub.

14 Pins \* 0.3 A = 4.2 A @ 5 Vdc  
4 Pins \* 0.3 A = 1.2 A @ 3.3 Vdc  
16 Pins \* 0.3 A = 4.8 A (GND)

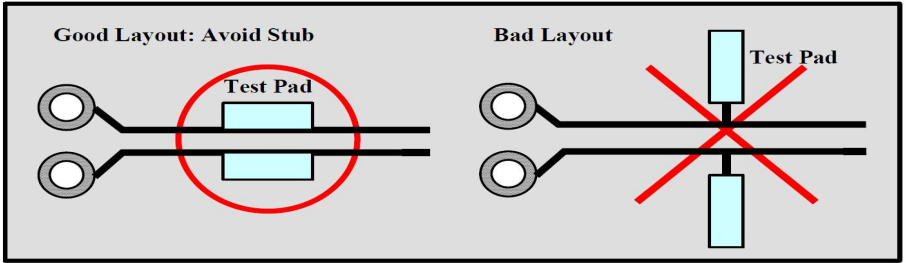
USB3\_RESET\_N = Reset USB 3.0 4 port hub.



Bottom Side  
System Test Points



Note: Some test points  
are on the respective  
pages of the signal



# Mechanical Holes and Shielding

